Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1 and 5 have been amended.

In item 4 of the above-identified Office Action, claims 1 - 6 and 8 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,981,179 to Shigemasa et al ("**SHIGEMASA**") in view of U. S. Patent No. 6,990,607 to Sim et al ("**SIM**"), and further in view of United States Patent No. 6,286,115 to Stubbs ("**STUBBS**"). In item 5 of the Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **SHIGEMASA** in view of **SIM** and **STUBBS**, and further in view of U. S. Patent Application Publication No. 2002/0066056 to Suzuki et al ("**SUZUKI**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

More particularly, claim 1 recites, among other limitations:

> **the microcontroller including a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective to calculate a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines**, said addresses being generated

> during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller, said addresses further being read out under control of said microcontroller, to outside of the integrated module. [emphasis added by Applicants]

Similarly, Applicants' claim 5 has been amended to recite, among other limitations:

> storing addresses of the memory cells of the memory which have been detected as defective during the functional testing **in a defect data memory in the microcontroller**, said addresses being stored in said defect data memory under control of said microcontroller **for use in calculating a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines;** [emphasis added by Applicants]

The defect data memory being part of the microcontroller on the integrated module under test is supported by the specification of the instant application, for example, page 10, lines 1 - 3, which state:

> **Parts of the microcontroller 3 include** a central processing unit (CPU) 4 and **an internal memory, which can be utilized as a command memory 5 and/or as a defect data memory 6**. [emphasis added by Applicants]

Additionally, as can be seen from the foregoing, Applicants' claimed invention stores the defect data in the defect memory of the microcontroller **for use in calculating a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines.**

Further, in Applicants' presently claimed invention, defect data is read to outside of the integrated module **only subsequent to the defect data being stored in the defect data memory of the microcontroller**. This can be seen, for example, in Applicants' claim 1 which recites, among other limitations:

> the microcontroller including a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective to calculate a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines, **said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller, said addresses further being read out under control of said microcontroller, to outside of the integrated module**. [emphasis added by Applicants]

Similarly, Applicants' claim 5 recites, among other limitations:

> **reading-out the addresses** of the memory cells of the memory which have been detected as defective during functional testing **stored in the defect data memory**, under the control of the microcontroller, **to outside the integrated module for further evaluation;** [emphasis added by Applicants]

As can be seen, in Applicants' claimed invention, the defect data is stored in a memory **that is part of the microcontroller on the integrated module under test.** Thus, Applicants' presently claimed invention makes it possible to carry out a self-test of an integrated module by using a microcontroller

and a data memory that is already integrated in the microcontroller, to carry out a normal operation of the integrated module. As such, in Applicants' claimed invention, no additional BIST hardware or additional on-chip test circuitry in necessary for this purpose.

Applicants' claimed invention is neither taught, nor suggested, by the prior art cited in the Office Action.

More particularly, page 4 of the Office Action acknowledges the failure of **SHIGEMASA**, stating, among other things, that:

> Shigemasa et al. does not explicitly teach the module comprising of a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller.

Additionally, page 4 of the Office Action acknowledges the further failures of the **SHIGEMASA** and **SIM** references, stating, among other things:

> Shigemasa et al. and Sim et al. does not explicitly teach redundant memory cells, said redundant memory cells being combined to form redundant row lines or redundant column lines and read out defect data used to calculate a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines.

In fact, the **SIM** reference fails to teach or suggest, among other limitations of Applicants' claims, memory cells arranged in row lines and column lines, as well as, using such defect data to calculate a repair solution. Rather, **SIM** discloses a mass data storage device, such as a disc drive, for storing a defect table including the index, head, cylinder, sector and span of a defect location. See, for example, Fig. 3 of **SIM**. As such, among other limitations of Applicants' claims, **SIM** fails to teach or suggest memory cells arranged in row lines and column lines. Additionally, the defect table of **SIM** is stored **in order to determine which portions of the recording medium of SIM are not to be used.** See, for example, col. 1 of **SIM**, lines 44 - 47, which state:

> The cached defect table is referred to by the microcontroller or microprocessor **to determine which portions of the recording medium <u>not to use</u>.**
> [emphasis added by Applicants]

In contrast to **SIM**, the present invention stores the defect data, and uses the stored defect data, **for <u>calculating a repair solution</u> to replace regular lines having defective memory cells with the redundant row lines or redundant column lines.** **SIM** fails to teach or suggest, among other limitations of Applicants' claims, using defect data stored in microcontroller memory to calculate a repair solution.

Page 5 of the Office Action goes on to allege that the elements of Applicants' former claim 1 missing from **SHIGEMASA** and **SIM** are disclosed in **STUBBS**. Applicants respectfully disagree.

As stated above, Applicants' amended claims require, among other limitations, storing addresses of memory cells detected as being defective during functional testing **in a defect data memory in the microcontroller, for use in calculating a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines.** However, this is not the case in **SHIGEMASA**, **SIM** or **STUBBS**. Rather, col. 4 of **STUBBS**, lines 31 – 34 state

> **When the query task 52 determines that the read data and the corresponding expect data do not agree, data describing the failed memory cell (e.g., the cell address) are written to a memory in the automated tester in a step 54.** When the query task 52 determines that the read data and the corresponding expect data do agree, control passes to a query task 56. [emphasis added by Applicants]

As such, the **STUBBS** reference clearly discloses storing data describing failed memory cells to a memory **in the external automated tester**, and not to a memory of the microcontroller on the integrated module under test, as required by Applicants' claims. As discussed in connection with those references, above, **SHIGEMASA** and **SIM references** do not cure the above-discussed deficiency of **STUBBS**. As such, the

combination of **SHIGEMASA**, **SIM** and **STUBBS** fails to teach or suggest all limitations of Applicants' claims. Further, moving the memory of **STUBBS** from the external tester to the microcontroller, as required by Applicants' claims, would impermissibly destroy the teachings of the **STUBBS** reference.

For the foregoing reasons, among others, it can be seen that Applicants' claims are patentable over the **SHIGEMASA**, **SIM** and **STUBBS** references, whether taken alone, or in combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5.

In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

For Applicants

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